UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,523	03/25/2004	Hiroyuki Hara	119243	5552

25944 7590 07/11/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
KRAMSKAYA, MARINA	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,523	HARA, HIROYUKI	
	Examiner	Art Unit	
	Marina Kramskaya	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/25/04, 8/06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I in the reply filed on 04/21/2005 is acknowledged. The traversal is on the ground(s) that the groups are not related as a combination and a subcombination. This is found persuasive, and the restriction requirement has been withdrawn. All claims 1-13 have been examined in this office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1-10 & 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morimura et al., US 6,438,257, in view of Yano, US 6,681,033

As per Claim 1, Morimura discloses a capacitance detection device (**2**) that reads asperity (column 6, lines 41-42) information for a subject surface by outputting a detection signal (from **40**) corresponding to the capacitance formed between the subject surface and the capacitance detection device, comprising:

a detection unit (**2**, FIG. 1) in which is arranged a plurality of capacitance detection circuits (sense units **1**, disposed in **2**) that output the detection signal; and

an amplification circuit (**30**, FIG. 2) that amplifies the detection signal,

wherein:

the capacitance detection circuit comprises a sensor electrode (**16**, as part of detection element **10**, FIG.3) for forming a capacitance (C_f) between the subject surface (finger **3**) and the sensor electrode (**16**) (column 6, lines 38-40), a signal output element (**40**) that outputs a detection signal corresponding to the capacitance (column 6, lines 48-53), and a low potential source (low level or **GND**) that connects to the signal transmission path (through N_{2a}) of the detection signal; and

the amplification circuit (**30**) functions as a signal source for outputting the detection signal to the capacitance detection circuit (column 6, lines 48-53) and is constituted such that the detection signal is transmitted from the amplification circuit (**30**) to the low potential source (low level or **GND**) via the signal output element (**40**).

Morimura does not explicitly disclose a low potential source line, which connects to the signal transmission path, or that a detection signal is transmitted from the amplification circuit to the low potential source line via the signal output element.

Yano discloses a low potential source line (**16**), which connects to the signal transmission path (13_{m+1}, 13_m, 13_{m-1}), and that a detection signal is transmitted from the amplification circuit (**OP**) to the low potential source line via (**16**) the signal output element (S_b).

Therefore, it would have been obvious to a person of ordinary skill in the art to a incorporate a low potential source line, which connects to the signal transmission path, and a detection signal that is transmitted from the amplification circuit to the low potential source line via the signal output element, as taught by Yano, in the capacitance sensing circuit of Morimura, in order to create a matrix of sensing elements to enhance the row and column sense line with parasitic capacitance (Yano: column 3, lines 3-30).

As per Claim 2, Morimura discloses the capacitance detection device according to claim 1, wherein:

the detection signal is a current signal (the detection signal is a current that is converted into voltage before the OUT stage: column 8, lines 31-34); and

the amplification circuit functions as a current source (i.e. the amplification circuit **30** supplies a current to the detection unit **40**, since there is no resistance to convert current to voltage) that supplies the current signal to the capacitance detection circuit (**40**).

As per Claim 3, Morimura discloses the capacitance detection device as applied to, claim 1. Morimura discloses forming the amplification circuit (**30**) outside the formation region of the detection unit (detection area **10**: see FIG. 3 for formation of detection area and the diagrams of FIG.'s 2 & 4, where the amplification unit is separate from the detection unit).

As per Claim 4, Morimura discloses the capacitance detection device as applied to claim 1, above.

Morimura does not disclose:

a plurality of select lines for selecting the capacitance detection circuit; and

a plurality of data lines for outputting the detection signal from the amplification circuit to the capacitance detection circuit,

the capacitance detection circuit further comprising a select transistor that connects to the respective select line and is constituted such that the passage and shutoff of electricity between the respective data line and signal output element is controlled by means of open/close control of the select transistor.

Yano discloses a capacitance detection device wherein:

a plurality of select lines (**12_{n+1}**, **12_n**, **12_{n-1}**) for selecting the capacitance detection circuit (plurality of **11**); and

a plurality of data lines (**13_{m+1}**, **13_m**, **13_{m-1}**) for outputting the detection signal from the amplification circuit (plurality of OP) to the capacitance detection circuit,

the capacitance detection circuit further comprises a select transistor (**S_r**) that connects to the respective select line (**12_{n+1}**, **12_n**, **12_{n-1}**) and is constituted such that the passage and shutoff of electricity between the respective data line (**13_{n+1}**, **13_n**, **13_{n-1}**) and signal output element is controlled by means of open/close control (ON/OFF states) of the select transistor (**S_r**).

Therefore, it would have been obvious to a person of ordinary skill in the art to use a plurality of select lines, a plurality of data lines, and select transistor, as taught by Yano, in the capacitance sensing device of Morimura, in order to create a matrix of sensing elements to enhance the row and column sense line with parasitic capacitance (Yano: column 3, lines 3-30).

As per Claims 5, Morimura further discloses the capacitance detection device, further comprising a pre-charging means (**PRE**) that pre-charge the data line as a stage prior (in stage **30**) to outputting (the Output stage **40**) the detection signal (OUT) on the data line.

As per Claim 6, Morimura further discloses the capacitance detection device, further comprising a pre-charge period (see PRE in FIG. 5A, period from 0 to first dashed line) setting means for setting the time between the pre-charge period, in which the pre-charging means execute data-line pre-charging (pre-charging occurs in the period from 0 to first dashed line in FIG. 5A: column 7, lines 44-48), and the sensing period (**Δt**: FIG. 5C), in which the signal output element outputs the detection signal (OUT). Morimura does not explicitly disclose setting a ratio. However, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to set a ratio based on a known time relationship for comparison between measurements in only one value instead of two for simplicity.

As per Claim 7, Morimura discloses the capacitance detection device as applied to claim 1, above. Morimura further discloses the capacitance detection device wherein:

the signal output element (**40**) is constituted as a three-terminal transistor (Q_{4a}) having a current control terminal (Drain), a current input terminal (Gate), and a current output terminal (Source), and further comprises potential control means (by Q_{1a} and Q_{2a} in amplifier stage **30**) for controlling the potential (input potential at Gate) as a stage prior to outputting the detection signal (amplifier stage **30**) corresponding to the capacitance (C_f), see Potential output curve (FIG. 5C) at node N_{2a}, the gate input node.

As per Claim 8, Morimura discloses the capacitance detection device as applied to claim 1. Morimura discloses a further capacitance detection embodiment wherein:

the capacitance detection circuit further comprises a reference capacitance (C_r, **51**) fixed capacitance value (i.e. set to a value within a predetermined range: column 9, lines 57-62); and

the signal output element outputs a detection signal that corresponds to the capacitance of the capacitance and the reference capacitance (see FIG. 21, which shows that change in capacitance). Morimura does not explicitly disclose setting a ratio. However, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to calculate the ratio from the capacitance results in the graph for comparison between measurements in only one value instead of two for simplicity.

As per Claim 9, Morimura discloses the capacitance detection device as applied to claim 1, above. Morimura further discloses forming the capacitance detection circuit on an insulating substrate (i.e. insulating layer **12** on substrate **11**, see FIG. 3).

As per Claims 10, Morimura discloses a fingerprint sensor (FIG. 1) that comprises the capacitance detection device according to claim 1, and is constituted to read fingerprint (of finger **3**) asperity information (column 6, lines 41-47).

As per Claim 12, Morimura discloses a drive method for a capacitance detection device that comprises a current amplification element (**10**) that increases or reduces the gain of a current signal in response to the capacitance (C_f) formed between the capacitance detection device (electrode **16**, in detection element **10**) and a subject surface (finger **3**); a data line (line between points N_{1a} and N_{2a}) for supplying the current signal (**I**, **21a**) to the current amplification element (**30**); an amplification circuit (**30**) that amplifies the current signal flowing through the data line (line between points N_{1a} and N_{2a}), the drive method comprising the steps of:

pre-charging (via **PRE**) the data line to a predetermined potential (V_{DD}, see FIG. 5A);

allowing electrical conduction between the data line and the current amplification element by opening a transistor (Q_{1a}) after the data-line pre-charging is complete (column 7, lines 63-64);

and performing sensing by supplying a current signal from the amplification circuit to the current amplification element via the data line and amplifying the current signal by means of current gain that corresponds to the capacitance.

Morimura does not disclose:

a select transistor that controls the passage and shutoff of electricity between the data line and the current amplification element; and a low potential source line that connects to the output path of the current signal, the drive method comprising the steps of:

electrically shutting off the data line and the current amplification element from each other by closing the select transistor.

Yano discloses:

a select transistor ($\mathbf{S_r}$) that controls the passage and shutoff of electricity between the data line ($\mathbf{13_{m+1}}$, $\mathbf{13_m}$, $\mathbf{13_{m-1}}$) and the current amplification element (**OP**); and a low potential source line (**16**) that connects to the output path (at points $\mathbf{15_{m+1}}$, $\mathbf{15_m}$, $\mathbf{15_{m-1}}$) of the current signal, the drive method comprising the steps of:

electrically shutting off the data line ($\mathbf{13_{m+1}}$, $\mathbf{13_m}$, $\mathbf{13_{m-1}}$) and the current amplification element (**OP**) from each other by closing the select transistor ($\mathbf{S_r}$).

Therefore, it would have been obvious to a person of ordinary skill in the art to include a selection transistor to shutoff electricity between the amplification element and data line, as taught by Yano, in the capacitive detector drive method of Morimura, for the purpose of enhancing the sensitivity and simplifying the circuit (Yano: column 3, lines 31-40).

As per Claim 13, Morimura in view of Yano disclose the drive method for the capacitance detection device according to claim 12.

Morimura further discloses that the period for executing the pre-charging step (**PRE**, FIG. 5A) and the period for executing the sensing step (FIG. 5C) is variable (i.e. the time for transistor Q1a to turn OFF after pre-charge, is variable, see column 7, lines 63-65). Morimura does not explicitly disclose setting a ratio. However, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to take the ratio of the two periods, after they are known, for comparison between measurements in only one value instead of two for simplicity.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morimura and Yano as applied to claim 10 above, and further in view of Tartagni, US 6,320,394.

Morimura discloses a fingerprint sensor as applied to Claim 10, above.

Morimura does not explicitly disclose using the fingerprint sensor as a biometrics authentication device.

Tartagni discloses a biometrics authentication device (column 2, lines 30-34) that comprises a fingerprint (**18**) sensor (**1**).

Therefore, it would have been obvious to a person of ordinary skill in the art to use the fingerprint sensor as a biometrics authentication device, as taught by Tartagni,

with the capacitive fingerprint sensor of Morimura, for personal identification in security applications (Tartagni: column 2, lines 23-38).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kramer, US 6,512,381, Imai, US 6,448,790, and Miyasaka, US 2003/0222659, disclose a capacitive fingerprint detection unit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571)272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Marina Kramskaya
Examiner
Art Unit 2858

M. Kramskaya

MK

ANJAN DEB
PRIMARY EXAMINER